

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0039] beginning at page 13, line 5, with the following rewritten paragraph:

1 **[0039]** In addition, it is contemplated that the temperature stability of
2 switched variable capacitor 20, particularly in its minimum capacitance state
3 (transistor 14 off) is greatly improved by this invention. The relation of junction
4 capacitance C_j :

$$5 \quad C_j \propto \frac{1}{\sqrt{V_R + V_{bi}}}$$

6 indicates that as reverse bias voltage V_R increases, the dependence of junction
7 capacitance C_j on the built-in voltage V_{bi} decreases. The built-in voltage V_{bi} is
8 dependent on temperature, while the reverse bias voltage V_R applied by bias
9 transistors 18 can be regulated (by an on-chip voltage regulator, band-gap
10 reference circuit, or the like) to be stable with temperature. As a result, an
11 increase in the reverse bias voltage V_R can reduce the temperature sensitivity of
12 junction capacitance C_j . Because bias transistors 18 can apply a stable, high
13 magnitude, reverse bias voltage V_R to across the source/drain regions junctions of
14 transistor 14, the junction capacitance C_j can therefore be made significantly more
15 stable over temperature than according to conventional circuits. Stability of
16 parasitic capacitance C_p' over temperature thus translates into temperature
17 stability of the minimum capacitance C_{min} , which depends on parasitic capacitance
18 C_p' :

$$19 \quad C_{\min} = \frac{CC'_p}{2(C + C'_p)}$$

20 The capacitance of switched variable capacitor 20 in the minimum capacitance
21 state (transistor 14 off) is therefore rendered more stable by the present invention.